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APPLICATION NO	Fi	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/799,743 03/15/2004		03/15/2004	Kazuhiro Masuda	119096	9229	
25944	7590	03/15/2006	EXAMINER			
OLIFF &	BERRIDG	E, PLC	DICKEY, THOMAS L			
P.O. BOX						
ALEXANI	DRIA, VA	22320	ART UNIT	PAPER NUMBER		
				2826		

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	on No.	Applicant(s)				
		10/799,74	3	MASUDA, KAZUHIRO				
	Office Action Summary	Examiner		Art Unit				
	٨٠	Thomas L		2826				
 Period for	The MAILING DATE of this communication	appears on the	cover sheet with the c	orrespondence ac	idress			
A SHC THE M - Extens after S - If the p - If NO p - Failure Any re	PRIENT STATUTORY PERIOD FOR RELATIONS OF THIS COMMUNICATIONS IN THE PROPERTY OF THIS COMMUNICATIONS OF THIS COMMUNICATIONS OF THE PROPERTY OF	N. R 1.136(a). In no ever reply within the state riod will apply and wi atute, cause the apply	ent, however, may a reply be timutory minimum of thirty (30) day Il expire SIX (6) MONTHS from ication to become ABANDONE	nely filed s will be considered timel the mailing date of this c D (35 U.S.C. § 133).				
Status								
1) X  F	Responsive to communication(s) filed on 03	3/02/2006						
•		his action is n	on-final.					
3)□ \$	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Dispositio	on of Claims							
5)□ ( 6)⊠ ( 7)□ (	Claim(s) 1,2 and 5-9 is/are pending in the application.  4a) Of the above claim(s) is/are withdrawn from consideration.  Claim(s) is/are allowed.  Claim(s) 1,2 and 5-9 is/are rejected.  Claim(s) is/are objected to.  Claim(s) are subject to restriction and/or election requirement.							
Applicatio	on Papers							
10)⊠ T , , ,	The specification is objected to by the Examember in the drawing(s) filed on 15 March 2004 is/arch 2004 is/ar	e: a)⊠ accep the drawing(s) b rection is require	e held in abeyance. See ed if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 C	FR 1.121(d).			
Priority ur	nder 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.								
2)  Notice 3) Informa	s) of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) ation Disclosure Statement(s) (PTO-1449 or PTO/SB/ No(s)/Mail Date		4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ate	O-152)			

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## **DETAILED ACTION**

1. At the 2/22/06 personal interview it was agreed that Kurashima et al. 2002/0017710 failed to disclose each and every element of the claims, in that Kurashima et al.'s conductive member 28 reached to the top of, but not over (as required by claim 1 in line 14) the wall portion of Kurashima et al.'s insulating material 22. The 102(b) rejection over Kurashima et al. is withdrawn. Finality of the 12/02/05 action is withdrawn. The current action is made final in place of the 12/02/05 action.

# Claim Rejections - 35 USC § 102

**2.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2, and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by HANAOKA ET AL. (2001/0027011).

Hanaoka et al. discloses an electronic instrument comprising a circuit board comprising a plurality of semiconductor devices which are stacked, each of the semiconductor devices being electrically connected through conductive members 70, and each comprising a substrate 10; a electrode 14, the electrode 14 being formed on

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the substrate 10; a through-hole 50 being formed through the electrode 14 and the substrate 10 in a stacking direction of the electrode 14 and the substrate 10; a conductive member 70 being inserted into the through-hole 50; a insulating material 52 being disposed between the electrode 14 and the conductive member 70, the insulating material 52 including a wall portion (note, figure 9, showing the wall portion of upper hole 26 extending above electrode 14) located higher than at least the electrode 14; and at least a interlayer dielectric 12 being formed between the substrate 10 and the electrode 14, the through-hole 50 being formed in the interlayer dielectric 12, and surfaces of the interlayer dielectric 12 and substrate 10 in the through-hole 50 are formed to have a level difference in a boundary area between the substrate 10 and the interlayer dielectric 12; the conductive member 70 being formed over the wall portion of the insulating material 52 from the through-hole 50 and the conductive member 70 being connected with the electrode 14, wherein the insulating material 52 is formed to cover a upper surface of the electrode 14 and a surface in the through-hole 50, and includes a connection hole 58 (seen best in figure 6B) for connecting at least the electrode 14 with the conductive member 70 at a position differing from the through-hole 50, the wall portion being disposed between the connection hole 58 and the throughhole 50, the conductive member 70 functions as a connection terminal which secures electrical connection in a axial direction of the through-hole 50, and a part of the conductive member 70 projects outward from the through-hole 50 on a side of the

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substrate 10 opposite to the side on which the electrode 14 is formed. Note figures 6B, 9, 11, and paragraphs 0110-0126 of Hanaoka et al.

### Response to Arguments

3. Applicant's arguments with respect to claims 1,2, and 5-9 have been considered but are most in view of the new ground(s) of rejection.

#### Conclusion

**4.** THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey Patent Examiner Art Unit 2826 03/06